REMARKS

Applicant respectfully requests reconsideration and allowance of the present application based on the following remarks. In the Office Action claims 1-27 stand rejected under 35 U.S.C. 103(a). Claims 1-27 remain pending in the Application of which claims 1, 11, 21, 24 and 27 are independent claims. Applicants reassert previous arguments provided in prior responses and submit the following additional explications responsive to the Final Office Action.

The Rejections Based on MacLellan

In the Office Action, claims 1-3, 8-9, 11-13, 18-19, 21-22 and 24-25 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent No. 6,636,933 to MacLellan et al. (MacLellan) in view of U.S. Patent No. 5,394,551 to Holt et al. (Holt). Each of the independent claims requires a hardware semaphore unit. No combination of MacLellan and Holt teaches, suggests or renders obvious a hardware semaphore unit as recited in the claims.

Independent claims 1, 11, 21 and 24 require a resource controller and claim 27 requires a memory controller and a peripheral controller. The Examiner cites message network 260 in MacLellan as teaching each of these controllers. The Examiner is wrong. MacLellan describes message network 260 as follows:

> Suffice it to say here, however, that the front-end and back-end directors 180_1 -180_{32}, 200_1 -200_{32} control data transfer between the host computer/server 120 and the bank of disk drives 140 in response to messages passing between the directors 180_1 -180_{32}, 200_1 -200_{32} through the messaging network 260. The messages facilitate the data transfer between host computer/server 120 and the bank of disk drives 140 with such data passing through the global cache memory 220 via the data transfer section 240.

(col. 5, lines 14-22). Further, MacLellan explicitly teaches that messaging network 260 is operative independently of the data transfer section 240 (col. 5, lines 5-6). Therefore, messaging network 260 merely passes messages that are created elsewhere, which messages facilitate data transfer, and messaging network explicitly operates independently of data transfer section. Therefore, it should be readily apparent, that any reasonable reading of MacLellan precludes an interpretation that the messaging network 260 is capable of permitting processors to

simultaneously access resources (*see, e.g.* claim 1) because cited messaging network 260 plays no part in generating the content of the messages since it operates independently of data transfer.

Even accepting, *arguendo*, the Examiner's suggestion that messaging network 260 can be viewed as a resource controller for permitting access to resources, MacLellan provides no teaching of semaphore control of shared resources and teaches away from the need for such semaphore control. First, semaphores as described in MacLellan are explicitly used for communication signaling purposes and for the sole purpose of describing the content of a serial data stream (col. 14, lines 25-45). Specifically, MacLellan states that serial-to-parallel converters "convert between a serial stream of information (i.e., data, address, and control, Cyclic Redundancy Checks (CRCs), signaling semaphores, etc.)..." (MacLellan at Col. 14, lines 31-33). The MacLellan semaphores are explicitly taught as serial protocol semaphores embedded in a serial data transmission such that "first word 0 is shown to include protocol signaling (e.g. semaphore) and a terminating 'start-frame' indication." (MacLellan at col. 14, lines 43-45). MacLellan does not teach, in any manner, how these serial protocol semaphores would be created and used. Consequently, it cannot reasonably be said that MacLellan teaches, suggests or otherwise describes a semaphore unit for controlling or prioritizing access to resources.

Furthermore, the structure of the data storage system in MacLellan teaches away from the use of semaphores. MacLellan includes a global cache memory 220 from which processors 121_1-121_{32} request data. Only if a cache miss is encountered, are disk drives 141_1-141_{32} accessed. The use of a cache interposes data transfer section 240 between the processors and disk drives, thereby obviating the use of semaphores because each processor does not connect to each resource and contention is not physically possible (See MacLellan Fig. 20). In particular, only the data transfer section 240 can access bank of disk drives 140, eliminating the potential of conflict and contention. Thus, it would have been apparent to one of ordinary skill in the art, that MacLellan teaches away from the use of semaphores for controlling accesses to shared resources.

Applicants also note that claims 1, 11, 21 and 24 require a bus that connects to each processor and resource while claim 27 requires first and second busses that connect respective processors with corresponding sets of memory resources. Applicant respectfully submits that the MacLellan does not teach such bus and no citation is provided in the Office Action. Thus, MacLellan does not teach necessary elements of the claims as asserted by the Examiner and, because MacLellan teaches away from the use of semaphores in controlling access to shared resources, no motivation could have existed to combine MacLellan with any of the cited art in a manner that could reasonably be said to cure the deficiencies of MacLellan.

For at least these reasons, the rejections based on MacLellan and Holt are improper and should be withdrawn.

The Rejections Based on Srini

Claims 1-3 also stand rejected under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 5,053,942 to Srini (Srini). Applicants repeat that Srini never mentions the use of semaphores anywhere in its written description and, consequently, it is not reasonable to suggest that one of ordinary skill in the art would have been motivated to combine Srini and Holt to obtain a hardware semaphore unit. Srini teaches an arbiter that does not use traditional mechanisms for controlling access to a shared memory (Srini at col. 5, lines 21-35). Srini explicitly teaches access control based on an arbiter that is constructed as a tree of one-of-two arbiters employing a synchronous scheme (Srini at col. 5, lines 36-66). Srini teaches the importance of such a scheme in providing an arbiter that "must be impartial in the sense that it gives equal priority to the processors ..." and Srini further teaches the accrued advantage that "no single processor can dominate a memory module while others are waiting for the same module" (col. 5, lines 17-21). Since semaphores effectively "lock" a device for use by one processor, it is clear that one of ordinary skill in the art would not have been motivated to replace the arbiter of Srini with a semaphore-based scheme that would not perform as required by Srini. Existence of such motivation is even more improbable given that Holt does not even teach a hardware semaphore unit.

For at least these reasons, therefore, the rejections based on Srini and Holt are improper and should be withdrawn.

The Rejections Based on Goodwin

Claims 1-3, 8-9, 11-13, 18-19, 21-22 and 24-25 stand rejected under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 6,125,429 to Goodwin et al. (Goodwin) in view of Holt. Claim 27 stands rejected as allegedly being unpatentable over Goodwin in view of Holt and further in view of Official notice. Applicants repeat that Goodwin never mentions the use of semaphores anywhere in its written description and, consequently, it is not reasonable to suggest that one of ordinary skill in the art would have been motivated to combine Goodwin and Holt to obtain a hardware semaphore unit. More particularly, Goodwin teaches that a mapping operation resolves issues with stale data in cache memory whereby multiple processors can share a cache; Goodwin teaches a guarantee that "both the "fill" data and the "victim" data are from the same memory module and thus, there is no "latency" between the "fill" command and the "writeback" command for the "victim" data since the "fill" command establishes a hardwire connection between the CPU and the memory module" (col. 3, lines 56-61). Thus, Goodwin is not concerned with controlling access to the cache or resolving relative priorities of processors requesting access but teaches the selection of data source ***after*** access is granted. Goodwin relegates access control to an arbiter chip 14 and, as acknowledged by the Examiner, includes no discussion of contention (*see, e.g.*, col. 4, lines 26-35). Since contention of processors requesting access is unimportant to Goodwin and lies beyond the scope of Goodwin's teachings, no motivation could have existed to combine Goodwin with Holt to provide a hardware semaphore unit. The existence of such motivation is even more improbable given that Holt does not even teach a hardware semaphore unit.

For at least these reasons, the rejections based on MacLellan and Holt are improper and should be withdrawn.

The Rejections Based on Hiller

Claims 1-2, 11-12, 21 and 24 stand rejected under 35 U.S.C. 103 as allegedly being unpatentable over U.S. Patent No. 5,081,575 to Hiller et al. (Hiller) in view of Holt. Applicants repeat that Hiller never mentions the use of semaphores anywhere in its written description and it is not reasonable to suggest that one of ordinary skill in the art would have been motivated to combine Hiller and Holt to obtain a hardware semaphore unit.

Furthermore, and contrary to Examiner's assertion, Hiller explicitly teaches that arbitration is unnecessary, as for example in the passage:

> The control section of the switch determines which connections are made at any one time. Each PE provides its own portion of the control field to the crossbar switch on every memory access cycle. The set of all of the PE control fields determines the configuration of the switch during any given memory access cycle. The crossbar switch configuration is, therefore, predetermined at the time that the PE microcode algorithms are developed. ***This approach eliminates the need for arbitration of access*** to PMEM's during run time, thereby allowing the crossbar switch to operate at or near 100% efficiency.

(Paragraph spanning cols. 6 and 7). Clearly, Hiller has no use for semaphores and no motivation could have existed to combine Hiller and Holt. Existence of such motivation is even more improbable given that Holt does not teach a hardware semaphore unit.

For at least these reasons, the rejections based on Hiller and Holt are improper and should be withdrawn.

CONCLUSION

All objections and rejections having been addressed, and in view of the foregoing, the claims are believed to be in form for allowance, and such action is hereby solicited. The Examiner is kindly requested to contact the undersigned at the telephone number listed below if any points remain in issue which may be best resolved through a personal or telephone interview.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,
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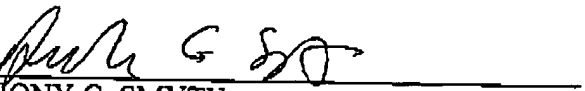

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